WHAT IS CLAIMED IS:

1. A non-volatile semiconductor memory device comprising:

a plurality of non-volatile memory cells each of which has a floating gate, a drain coupled to a bit line and a threshold voltage representing data of at least two bits, wherein electrons are capable of being injected into the floating gate, and wherein threshold voltages of the plurality of non-volatile memory cells are shiftable among at least three threshold levels which indicate mutually different programming states and which also differ from a threshold level indicating an erase state; and

sensing/program-verifying circuitry receiving a parameter which represents the threshold voltage of one non-volatile memory cell, a first programming reference parameter, a first read reference parameter, a second programming reference parameter, a second read reference parameter, a third programming reference parameter and a third read reference parameter;

wherein the first read reference parameter is allocated between the threshold level indicating the erase state and the first programming reference parameter, the

second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third programming reference parameter,

wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified that the one non-volatile memory cell threshold voltage has been shifted to that threshold level,

wherein the first programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a first threshold level of the three threshold levels, and the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indicating the erase state,

wherein the second programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a second threshold level of the three threshold levels, and the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level,

wherein the third programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a third threshold level of the three threshold levels, and the third read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level,

wherein the first read reference parameter, the second read reference parameter and the third read reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile memory cell can be read out as output data of a plurality of bits,

wherein the normal read operation includes parallel-comparing the parameter representing the threshold voltage of the one non-volatile memory cell with the plurality of read reference parameters using a plurality of sense

circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter representing the threshold voltage of the one non-volatile memory cell, a second input terminal of the first sense circuit is supplied with the first read reference parameter, a second input terminal of the second sense circuit is supplied with the second read reference parameter and a second input terminal of the third sense circuit is supplied with the third read reference parameter,

wherein an operation of shifting the threshold voltage of the one non-volatile memory cell to the threshold level indicating the selected programming state includes a program operation, in which electrons are injected into the floating gate of the one non-volatile memory cell using a programming voltage applied to the bit line coupled to the drain of the one non-volatile memory cell,

wherein the program operation includes a series of programming operations each followed by a related verifying operation, and

wherein the series of programming operations includes a first programming operation and a second programming operation after the first programming operation, the duration of the second programming operation beingshorter than that of the first programming operation.

2. The non-volatile semiconductor memory device according to claim 1,

wherein the first programming operation is carried out using the programming voltage of a single pulse, and the second programming operation is carried out using the programming voltage of a single pulse.

3. The non-volatile semiconductor memory device according to claim 1,

wherein the first programming operation is carried out using the programming voltage of a mono-pulse, and the second programming operation is carried out using the programming voltage of a mono-pulse.

4. The non-volatile semiconductor memory device according to claim 1,

wherein each said verifying operation verifies whether the threshold voltage of the one non-volatile multi-level memory cell has been shifted to the threshold level indicating the selected programming state, and includes comparing the parameter representing the threshold voltage of the one non-volatile multi-level memory cell with the programming reference parameter corresponding to the selected programming state.

5. The non-volatile semiconductor memory device according to claim 1,

wherein the operation of shifting the threshold voltage includes an erasure operation in which non-volatile multi-level memory cells of one of a byte, a block and a chip level can be erased.

6. The non-volatile semiconductor memory device according to claim 1,

wherein each of the plurality of non-volatile multi-level memory cells has a control gate, and a control gate of a memory cell to be programmed is supplied with a predetermined potential which is different from a potential being supplied to a control gate of a non-selected cell.

7. A non-volatile semiconductor memory device comprising:

a plurality of non-volatile memory cells each of which has a floating gate, a drain coupled to a bit line and a threshold voltage representing data of at least two bits, wherein electrons are capable of being injected into the floating gate, and wherein threshold voltages of the plurality of non-volatile memory cells are shiftable among at least three threshold levels which indicate mutually different programming states and which also differ from a threshold level indicating an erase state; and

sensing/program-verifying circuitry receiving a parameter which represents the threshold voltage of one non-volatile memory cell, a first programming reference parameter, a first read reference parameter, a second programming reference parameter, a second read reference parameter, a third programming reference parameter and a third read reference parameter;

wherein the first read reference parameter is allocated between the threshold level indicating the erase state and the first programming reference parameter, the second read reference parameter is allocated between the

first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third programming reference parameter,

wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified that the one non-volatile memory cell threshold voltage has been shifted to that threshold level,

wherein the first programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a first threshold level of the three threshold levels, and the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indicating the erase state,

wherein the second programming reference parameter is used for verifying whether non-volatile memory cell

threshold voltages are shifted to a second threshold level of the three threshold levels, and the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level,

wherein the third programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a third threshold level of the three threshold levels, and the third read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level,

wherein the first read reference parameter, the second read reference parameter and the third read reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile memory cell can be read out as output data of a plurality of bits,

wherein the normal read operation includes parallel-comparing the parameter representing the threshold voltage of the one non-volatile memory cell with the plurality of read reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input

terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter representing the threshold voltage of the one non-volatile memory cell, a second input terminal of the first sense circuit is supplied with the first read reference parameter, a second input terminal of the second sense circuit is supplied with the second read reference parameter and a second input terminal of the third sense circuit is supplied with the third read reference parameter,

wherein an operation of shifting the threshold voltage of the one non-volatile memory cell to the threshold level indicating the selected programming state includes a program operation, in which electrons are injected into the floating gate of the one non-volatile memory cell using a programming voltage applied to a control gate of the one non-volatile memory cell,

wherein the program operation includes a series of programming operations each followed by a related verifying operation, and

wherein the series of programming operations includes a first programming operation and a second programming operation after the first programming operation, the

duration of the second programming operation being shorter than that of the first programming operation.

8. The non-volatile semiconductor memory device according to claim 7,

wherein the first programming operation is carried out using the programming voltage of a single pulse, and the second programming operation is carried out using the programming voltage of a single pulse.

9. The non-volatile semiconductor memory device according to claim 7,

wherein the first programming operation is carried out using the programming voltage of a mono-pulse, and the second programming operation is carried out using the programming voltage of a mono-pulse.

10. The non-volatile semiconductor memory device according to claim 7,

wherein each said verifying operation verifies whether the threshold voltage of the one non-volatile multi-level memory cell has been shifted to the threshold level indicating the selected programming state, and includes

comparing the parameter representing the threshold voltage of the one non-volatile multi-level memory cell with the programming reference parameter corresponding to the selected programming state.

11. The non-volatile semiconductor memory device according to claim 7,

wherein the operation of shifting the threshold voltage includes an erasure operation in which non-volatile multi-level memory cells of one of a byte, a block and a chip level can be erased.

12. The non-volatile semiconductor memory device according to claim 7,

wherein each of the plurality of non-volatile multi-level memory cells has a control gate, and a control gate of a memory cell to be programmed is supplied with a predetermined potential which is different from a potential being supplied to a control gate of a non-selected cell.

13. A non-volatile semiconductor memory device comprising:

a plurality of non-volatile memory cells each of which has a floating gate, a drain coupled to a bit line and a threshold voltage representing data of at least two bits, wherein electrons are capable of being injected into the floating gate, and wherein threshold voltages of the plurality of non-volatile memory cells are shiftable among at least three threshold levels which indicate mutually different programming states and which also differ from a threshold level indicating an erase state; and

sensing/program-verifying circuitry receiving a parameter which represents the threshold voltage of one non-volatile memory cell, a first programming reference parameter, a first read reference parameter, a second programming reference parameter, a second read reference parameter, a third programming reference parameter and a third read reference parameter;

wherein the first read reference parameter is allocated between the threshold level indicating the erase state and the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second

programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third programming reference parameter,

wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified that the one non-volatile memory cell threshold voltage has been shifted to that threshold level,

wherein the first programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a first threshold level of the three threshold levels, and the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indicating the erase state,

wherein the second programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a second threshold level

of the three threshold levels, and the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level,

wherein the third programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a third threshold level of the three threshold levels, and the third read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level,

wherein the first read reference parameter, the second read reference parameter and the third read reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile memory cell can be read out as output data of a plurality of bits,

wherein the normal read operation includes parallel-comparing the parameter representing the threshold voltage of the one non-volatile memory cell with the plurality of read reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense

circuit and the third sense circuit are commonly supplied with the parameter representing the threshold voltage of the one non-volatile memory cell, a second input terminal of the first sense circuit is supplied with the first read reference parameter, a second input terminal of the second sense circuit is supplied with the second read reference parameter and a second input terminal of the third sense circuit is supplied with the third read reference parameter,

wherein an operation of shifting the threshold voltage of the one non-volatile memory cell to the threshold level indicating the selected programming state includes a program operation, in which electrons are injected into the floating gate of the one non-volatile memory cell using a programming voltage applied to the bit line coupled to the drain of the one non-volatile memory cell,

wherein the program operation includes a series of programming operations each followed by a related verifying operation,

wherein the series of programming operations includes a first programming operation and a second programming operation after the first programming operation, and

wherein a parameter of the first programming operation has a first predetermined value and a same parameter of the second programming operation has a second predetermined value different from the first predetermined value so that a first threshold voltage change of the one non-volatile multi-level memory cell caused by the first programming operation is substantially larger than a second threshold voltage change of the one non-volatile multi-level memory cell caused by the second programming operation.

14. The non-volatile semiconductor memory device according to claim 13,

wherein the parameter of the first and the second programming operations includes a duration of the respective programming operation.

15. The non-volatile semiconductor memory device according to claim 13,

wherein the first programming operation is carried out using the programming voltage of a single pulse, and the second programming operation is carried out using the programming voltage of a single pulse.

16. The non-volatile semiconductor memory device according to claim 13,

wherein the first programming operation is carried out using the programming voltage of a mono-pulse, and the second programming operation is carried out using the programming voltage of a mono-pulse.

17. The non-volatile semiconductor memory device according to claim 13,

wherein each said verifying operation verifies whether the threshold voltage of the one non-volatile multi-level memory cell has been shifted to the threshold level indicating the selected programming state, and includes comparing the parameter representing the threshold voltage of the one non-volatile multi-level memory cell with the programming reference parameter corresponding to the selected programming state

18. The non-volatile semiconductor memory device according to claim 13,

wherein the operation of shifting the threshold voltage includes an erasure operation in which non-volatile

multi-level memory cells of one of a byte, a block and a chip level can be erased.

19. The non-volatile semiconductor memory device according to claim 13,

wherein each of the plurality of non-volatile multi-level memory cells has a control gate, and a control gate of a memory cell to be programmed is supplied with a predetermined potential which is different from a potential being supplied to a control gate of non-selected cell.

20. A non-volatile semiconductor memory device comprising:

a plurality of non-volatile memory cells each of which has a floating gate, a drain coupled to a bit line and a threshold voltage representing data of at least two bits, wherein electrons are capable of being injected into the floating gate, and wherein threshold voltages of the plurality of non-volatile memory cells are shiftable among at least three threshold levels which indicate mutually different programming states and which also differ from a threshold level indicating an erase state; and

sensing/program-verifying circuitry receiving a parameter which represents the threshold voltage of one non-volatile memory cell, a first programming reference parameter, a first read reference parameter, a second programming reference parameter, a second read reference parameter, a third programming reference parameter and a third read reference parameter;

wherein the first read reference parameter is allocated between the threshold level indicating the erase state and the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third programming reference parameter,

wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified that the one non-

volatile memory cell threshold voltage has been shifted to that threshold level,

wherein the first programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a first threshold level of the three threshold levels, and the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indicating the erase state,

wherein the second programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a second threshold level of the three threshold levels, and the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level,

wherein the third programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a third threshold level of the three threshold levels, and the third read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level,

wherein the first read reference parameter, the second read reference parameter and the third read reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile memory cell can be read out as output data of a plurality of bits,

wherein the normal read operation includes parallel-comparing the parameter representing the threshold voltage of the one non-volatile memory cell with the plurality of read reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter representing the threshold voltage of the one non-volatile memory cell, a second input terminal of the first sense circuit is supplied with the first read reference parameter, a second input terminal of the second sense circuit is supplied with the second read reference parameter and a second input terminal of the third sense circuit is supplied with the third read reference parameter,

wherein an operation of shifting the threshold voltage of the one non-volatile memory cell to the threshold level

indicating the selected programming state includes a program operation, in which electrons are injected into the floating gate of the one non-volatile memory cell using a programming voltage applied to a control gate of the one non-volatile memory cell,

wherein the program operation includes a series of programming operations each followed by a related verifying operation,

wherein the series of programming operations includes a first programming operation and a second programming operation after the first programming operation, and

wherein a parameter of the first programming operation has a first predetermined value and a same parameter of the second programming operation has a second predetermined value different from the first predetermined value so that a first threshold voltage change of the one non-volatile multi-level memory cell caused by the first programming operation is substantially larger than a second threshold voltage change of the one non-volatile multi-level memory cell caused by the second programming operation.

21. The non-volatile semiconductor memory device according to claim 20,

wherein the parameter of the first and the second programming operations includes a duration of the respective programming operation.

22. The non-volatile semiconductor memory device according to claim 20,

wherein the first programming operation is carried out using the programming voltage of a single pulse, and the second programming operation is carried out using the programming voltage of a single pulse.

23. The non-volatile semiconductor memory device according to claim 20,

wherein the first programming operation is carried out using the programming voltage of a mono-pulse, and the second programming operation is carried out using the programming voltage of a mono-pulse.

24. The non-volatile semiconductor memory device according to claim 20,

wherein each said verifying operation verifies whether the threshold voltage of the one non-volatile multi-level memory cell has been shifted to the threshold level

indicating the selected programming state, and includes comparing the parameter representing the threshold voltage of the one non-volatile multi-level memory cell with the programming reference parameter corresponding to the selected programming state.

25. The non-volatile semiconductor memory device according to claim 20,

wherein the operation of shifting the threshold voltage includes an erasure operation in which non-volatile multi-level memory cells of one of a byte, a block and a chip level can be erased.

26. The non-volatile semiconductor memory device according to claim 20,

wherein each of the plurality of non-volatile multi-level memory cells has a control gate, and a control gate of a memory cell to be programmed is supplied with a predetermined potential which is different from a potential being supplied to a control gate of non-selected cell.

27. A non-volatile semiconductor memory device comprising:

a plurality of non-volatile memory cells each of which has a control gate, a floating gate, a drain coupled to a bit line and a threshold voltage representing data of at least two bits, wherein electrons are capable of being injected into the floating gate, and wherein threshold voltages of the plurality of non-volatile memory cells are shiftable among at least three threshold levels which indicate mutually different programming states and which also differ from a threshold level indicating an erase state; and

sensing/program-verifying circuitry receiving a parameter which represents the threshold voltage of one non-volatile memory cell, a first programming reference parameter, a first read reference parameter, a second programming reference parameter, a second read reference parameter, a third programming reference parameter and a third read reference parameter;

wherein the first read reference parameter is allocated between the threshold level indicating the erase state and the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read

reference parameter is allocated between the second programming reference parameter and the third programming reference parameter,

wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified that the one non-volatile memory cell threshold voltage has been shifted to that threshold level,

wherein the first programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a first threshold level of the three threshold levels, and the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indicating the erase state,

wherein the second programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a second threshold level of the three threshold levels, and the second read

reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level,

wherein the third programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a third threshold level of the three threshold levels, and the third read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level,

wherein the first read reference parameter, the second read reference parameter and the third read reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile memory cell can be read out as output data of a plurality of bits,

wherein the normal read operation includes parallel-comparing the parameter representing the threshold voltage of the one non-volatile memory cell with the plurality of read reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied

with the parameter representing the threshold voltage of the one non-volatile memory cell, a second input terminal of the first sense circuit is supplied with the first read reference parameter, a second input terminal of the second sense circuit is supplied with the second read reference parameter and a second input terminal of the third sense circuit is supplied with the third read reference parameter,

wherein an operation of shifting the threshold voltage of the one non-volatile memory cell to the threshold level indicating the selected programming state includes a program operation, in which electrons are injected into the floating gate of the one non-volatile memory cell using programming voltages applied to the bit line and the control gate, respectively,

wherein the program operation includes a series of programming operations each followed by a related verifying operation, and

wherein the series of programming operations includes a first programming operation and a second programming operation after the first programming operation, the duration of the second programming operation being shorter than that of the first programming operation.

28. The non-volatile semiconductor memory device according to claim 27,

wherein the first programming operation is carried out using the programming voltage of a single pulse, and the second programming operation is carried out using the programming voltage of a single pulse.

29. The non-volatile semiconductor memory device according to claim 27,

wherein the first programming operation is carried out using the programming voltage of a mono-pulse, and the second programming operation is carried out using the programming voltage of a mono-pulse.

30. The non-volatile semiconductor memory device according to claim 27,

wherein each said verifying operation verifies whether the threshold voltage of the one non-volatile multi-level memory cell has been shifted to the voltage threshold level indicating the selected programming state, and includes comparing the parameter representing the threshold voltage of the one non-volatile multi-level memory cell with the

programming reference parameter corresponding to the selected programming state.

31. The non-volatile semiconductor memory device according to claim 27,

wherein the operation of shifting the threshold voltage includes an erasure operation in which non-volatile multi-level memory cells of one of a byte, a block and a chip level can be erased.

32. The non-volatile semiconductor memory device according to claim 27,

wherein the control gate of a memory cell to be programmed is supplied with a predetermined potential which is different from a potential being supplied to the control gate of a non-selected cell.

33. A non-volatile semiconductor memory device comprising:

a plurality of non-volatile memory cells each of which has a control gate, a floating gate, a drain coupled to a bit line and a threshold voltage representing data of at least two bits, wherein electrons are capable of being

injected into the floating gate, and wherein threshold voltages of the plurality of non-volatile memory cells are shiftable among at least three threshold levels which indicate mutually different programming states and which also differ from a threshold level indicating an erase state; and

sensing/program-verifying circuitry receiving a parameter which represents the threshold voltage of one non-volatile memory cell, a first programming reference parameter, a first read reference parameter, a second programming reference parameter, a second read reference parameter, a third programming reference parameter and a third read reference parameter;

wherein the first read reference parameter is allocated between the threshold level indicating the erase state and the first programming reference parameter, the second read reference parameter is allocated between the first programming reference parameter and the second programming reference parameter, and the third read reference parameter is allocated between the second programming reference parameter and the third programming reference parameter,

wherein the sensing/program-verifying circuitry generates data of at least two bits represented by the one non-volatile memory cell threshold voltage, verifies whether the one non-volatile memory cell threshold voltage is shifted to the threshold level indicating a selected one of the programming states, and programs the one non-volatile memory cell until it is verified that the one non-volatile memory cell threshold voltage has been shifted to that threshold level,

wherein the first programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a first threshold level of the three threshold levels, and the first read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the first threshold level or to the threshold level indicating the erase state,

wherein the second programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a second threshold level of the three threshold levels, and the second read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the second threshold level or to the first threshold level,

wherein the third programming reference parameter is used for verifying whether non-volatile memory cell threshold voltages are shifted to a third threshold level of the three threshold levels, and the third read reference parameter is used for detecting whether non-volatile memory cell threshold voltages are near to the third threshold level or to the second threshold level,

wherein the first read reference parameter, the second read reference parameter and the third read reference parameter are parameters for a normal read operation in which the information stored in the one non-volatile memory cell can be read out as output data of a plurality of bits,

wherein the normal read operation includes parallel-comparing the parameter representing the threshold voltage of the one non-volatile memory cell with the plurality of read reference parameters using a plurality of sense circuits including at least a first sense circuit, a second sense circuit and a third sense circuit, first input terminals of the first sense circuit, the second sense circuit and the third sense circuit are commonly supplied with the parameter representing the threshold voltage of the one non-volatile memory cell, a second input terminal of the first sense circuit is supplied with the first read

reference parameter, a second input terminal of the second sense circuit is supplied with the second read reference parameter and a second input terminal of the third sense circuit is supplied with the third read reference parameter,

wherein an operation of shifting the threshold voltage of the one non-volatile memory cell to the threshold level indicating the selected programming state includes a program operation, in which electrons are injected into the floating gate of the one non-volatile memory cell using programming voltages applied to the bit line and the control gate, respectively,

wherein the program operation includes a series of programming operations each followed by a related verifying operation,

wherein the series of programming operations includes a first programming operation and a second programming operation after the first programming operation, and

wherein a parameter of the first programming operation has a first predetermined value and a same parameter of the second programming operation has a second predetermined value different from the first predetermined value so that a first threshold voltage change of the one non-volatile

multi-level memory cell caused by the first programming operation is substantially larger than a second threshold voltage change of the one non-volatile multi-level memory cell caused by the second programming operation.

34. The non-volatile semiconductor memory device according to claim 33,

wherein the parameter of the first and the second programming operations includes a duration of the respective programming operation.

35. The non-volatile multi-level memory according to claim 33,

wherein the first programming operation is carried out using the programming voltage of a single pulse, and the second programming operation is carried out using the programming voltage of a single pulse.

36. The non-volatile multi-level memory device according to claim 33,

wherein the first programming operation is carried out using the programming voltage of a mono-pulse, and the

second programming operation is carried out using the programming voltage of a mono-pulse.

37. The non-volatile multi-level memory device according to claim 33,

wherein each said verifying operation verifies whether the threshold voltage of the one non-volatile multi-level memory cell has been shifted to the threshold voltage level indicating the selected programming state, and includes comparing the parameter representing the threshold voltage of the one non-volatile multi-level memory cell with the programming reference parameter corresponding to the selected programming state.

38. The non-volatile semiconductor memory device according to claim 33,

wherein the operation of shifting the threshold voltage includes an erasure operation in which non-volatile multi-level memory cells of one of a byte, a block and a chip level can be erased.

39. The non-volatile semiconductor memory device according to claim 33,

wherein the control gate of a memory cell to be programmed is supplied with a predetermined potential which is different from a potential being supplied to the control gate of non-selected cell.

40. The non-volatile semiconductor memory device according to claim 1,

wherein the program operation includes a verify operation before the series of the programming operations.

41. The non-volatile semiconductor memory device according to claim 7,

wherein the program operation includes a verify operation before the series of the programming operations.

42. The non-volatile semiconductor memory device according to claim 13,

wherein the program operation includes a verify operation before the series of the programming operations.

43. The non-volatile semiconductor memory device according to claim 20,

wherein the program operation includes a verify operation followed by the series of the programming operations.

44. The non-volatile semiconductor memory device according to claim 27,

wherein the program operation includes a verify operation followed by the series of the programming operations.